Modulation Techniques for All-Digital Transmitters based on Pulse Direct Digital Synthesizers

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***Abstract*—Purely digital RF Transmitters of minimal footprint and power consumption and of acceptable performance for a wide range of applications are built out of Pulse Direct Digital frequency Synthesizers with spurs-suppression dithering and modulation capability. Several basic modulation schemes (FM / FSK / PM / PSK / AM / ASK) applied to Pulse Direct Digital frequency Synthesizers are considered.**

I. INTRODUCTION

Pulse Direct Digital Synthesizer (PDDS) is a compact and minimalistic Direct All Digital Synthesizer architecture [1]. It is a simplified version of the standard DDS core [2] as it does not have either a Sine Table or a Digital to Analog converter. It only consists of the phase accumulator (of n bits wide), the Most Significant Bit (MSB) of which is used as the output (Fig. 1). The *average* output frequency, $f_{ave} = \frac{w}{2^n} \cdot f_{clk}$, where w (n-1 bits) is the value of the Frequency Control Word (FCW) and f_{clk} is the reference clock, ranges within (0 , f_{clk} /2) typically with very high resolution.

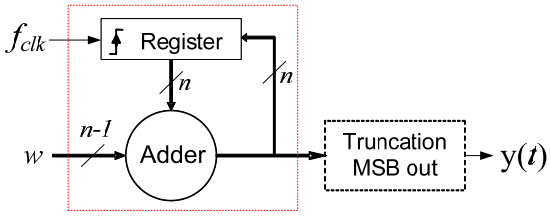

Figure 1. Pulse Direct Digital Synthesizer core.

In addition to the generated carrier signal (of *average* output frequency f_{ave}) the output of the PDDS contains many strong and undesired frequency spurs. To suppress them, Frequency and Phase Dithering, both purely digital techniques, ban be used [3]. Phase Dithering is applied to the PDDS by adding a random number sequence to the output of the Phase Accumulator (just before the MSB truncation that gives the final 1-bit output).

It has been shown in [4] that using the appropriate random number sequence for the phase dithered PDDS, a spurs-free output can be generated as shown in Fig. 2. The drawback of the dithering methods is the resulting noise floor which however depends on the rate of the reference clock f_{clk} (or the maximum operating frequency of its implementation).

$$NoiseFloor = \left[10\log_{10}\left(f_{clk}\right) - 3\right] \quad \text{dBc/Hz} \qquad (1)$$

It can be shown that the noise floor level is given by Eq. (1) and so a high-end ASIC implementation can easily achieve a noise floor of 90dBc/Hz. Such performance may not be appropriate for high-end RF applications, but this architecture is very useful for low-power, low-cost, fully reconfigurable and short range applications.

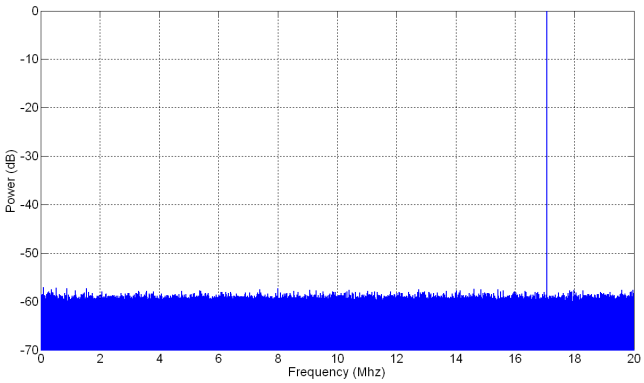

Figure 2. Spectrum of a phase dithered PDDS using the random sequence proposed in [] (Matlab, f_{clk} = 40Mhz).

To get a complete All-Digital transmitter architecture we introduce the basic modulation schemes (FM / FSK / PM / PSK / AM / ASK) applied to this PDDS architecture. Combining these basic schemes more advanced modulation schemes (QAM ect) can be realized.

The most challenging is the AM / ASK modulation and this paper presents various alternative implementations of it which not only achieve the desired modulation but further decrease the noise floor level (compared to Eq. 1) as well.

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Finally various implementation examples and an AM radio transmitter based on these techniques are presented.

II. FM / FSK / PM / PSK MODULATED PDDS

FM and PM modulation schemes for the PDDS are derived directly from their DDS equivalent ones [5]. The FM / FSK modulation is implemented by adding the data stream we want to transmit to the FCW (Fig. 3). As in all cases of FM / FSK modulation the amplitude of the data stream should be a small fraction of the FCW (e.g. we could represent the data stream using p-bit words with $p<<n$). Another typical requirement for the data stream is to be of singed form with zero mean value so that it does not affect the average generated frequency. Furthermore, one can impose to the data stream other spectral requirements according to the specifications the transmitter needs to satisfy.

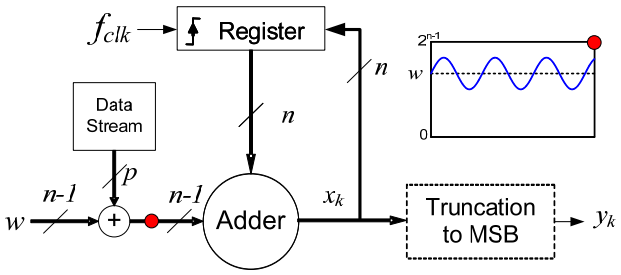

Figure 3. FM / FSK modulated PDDS core.

The PDDS's Phase Accumulator output of n-bit has the phase information of the generated signal so we can do PM / PSK modulation by adding the data stream to it as shown in Fig. 4. If needed the data stream can be converted into an n-bit signal (before adding) by inserting zeros to the LSB positions. Doing so, the whole 360° of phase range can be used in equally spaced modulation steps.

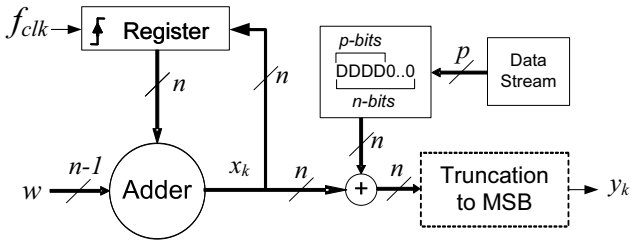

Figure 4. PM / PSK modulated PDDS core.

Based on this modulation scheme an 8PSK demo has been implemented within a Xilinx Spartan 3e FPGA evaluation board. The design achieved an operating frequency f_{clk} of 200 Mhz. Fig. 5 presents the constellation of the generated signal. For this measurement the carrier frequency was randomly selected to be 95.1296Mhz while the symbol rate of the 8PSK modulation was 1M symbol/sec.

These techniques can be combined with phase dithering and result in a fully reconfigurable and spurs-free modulated frequency synthesizer. Such an FM / FSK / PM / PSK synthesizer with a digital data input has also been implemented in a 90nm CMOS technology. The synthesizer occupied a chip area of 500um x 100um (including power ring and decupling) and achieves an operating of 2Ghz.

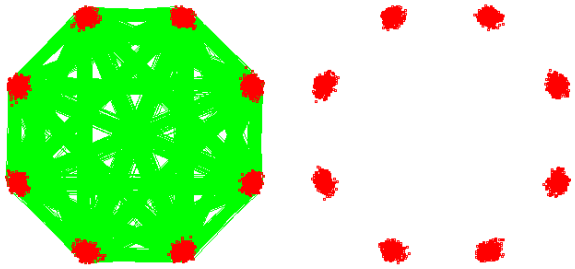

Figure 5. 8PSK FPGA implementation demo constellation.

III. AM / ASK MODULATION

While FM and PM modulations are easily implemented on a PDDS core, the AM modulation is more challenging to realize while having 1-bit digital output as before (and so having no analog components like DACs etc.). In this section we examine two main ways to do AM modulation; the first one is simple and can be combined easily with FM or PM modulation but uses two resistors at the output to mix the signals of two digital sources and produce a three-level output ; the second one is more involved but produces digital output.

A. Dual phase output method

The first method, originally presented in [6], can be implemented using the PDDS. The main idea is to use a modified phase-dithered PDDS core to produce two output signals of the same frequency but of different phase $d(t)$. The information of the data stream $s(t)$ in encoded into the phase difference $d(t)$. Then, the two 1-bit generated signals are added by an analog network of two resistors to generate the AM modulated signal (Fig. 6). The technique is based on Eq. (2) and a data encoding of the form $d(t)=2\cdot\arccos(s(t)/2)$.

$$\begin{aligned}\sin(\omega t)+\sin(\omega t+d(t)) &= 2\cos(d(t)/2)\cdot\sin(\omega t+d(t)/2)\\ &= s(t)\cdot\sin(\omega t+d(t)/2)\end{aligned} \quad (2)$$

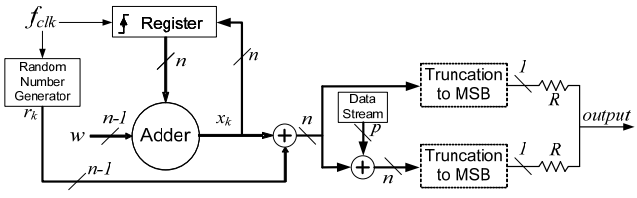

Figure 6. Simple PDDS-based dual-phase AM modulation scheme.

While this technique is not actually more hardware complex that a simple PM modulated PDDS, it has a drawback. According to Eq. (2) the values of the data stream d not only modulate the amplitude but the phase of the generated signal as well. This topology is not convenient to use in combination with other modulation schemes (e.g. PM,

FM). Instead, the variation in Fig. 7 does not have this problem; it is however slightly more complex.

In Fig. 7 the data stream $s(t)$ differentially modulates the phases of the two paths by $d(t)=\arccos(s(t)/2)$ so that adding them results in a purely AM modulated signal according to the following equation:

$$\begin{aligned}\sin(\omega t+d(t))+\sin(\omega t-d(t)) &= 2\cos(d(t))\cdot\sin(\omega t)\\ &= s(t)\cdot\sin(\omega t)\end{aligned} \quad . \quad (3)$$

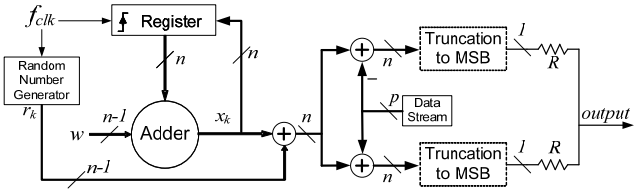

Figure 7. PDDS-based differential-phase AM modulation topology.

The above topologies implement the AM / ASK modulation scheme with minimal hardware overhead. However, although they use a 3-level output to synthesize the signal, they still have the typical noise floor performance of the phase dithered PDDS, (1).

The topology in Fig. 8 instead takes advantage of the 3-level output to further reduce the output noise floor by 3dB/Hz. Here, phase dithering is not applied directly to the output of the Phase Accumulator but instead on each of the two generated phases independently. For each phase a different (and independent) random number generator is used.

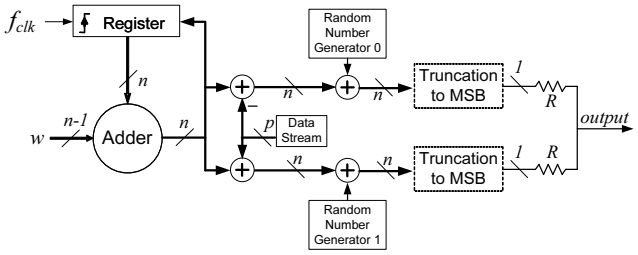

Figure 8. PDDS-based differential-phase AM modulation topology using two independent dithering sources.

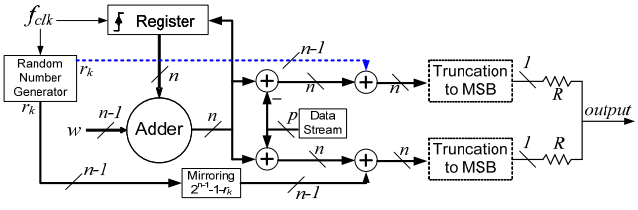

Figure 9. PDDS-based differential-phase AM modulation topology using dithering sequence mirroring.

Finally, the variation in Fig. 9 achieves a noise floor improvement of up to 6dB/Hz using less hardware as well. Here a single random number generator is used. Its output dithers directly the one of the phases while the other phase is dithered by the complementary $\overline{r_k}=2^{n-1}-1-r_k=\left(2^{n-1}-1\right)\otimes r_k$. This way part of the noise introduced by phase dithering process is cancelled out by the analog addition network.

B. Amplitude multiplication technique

This technique can be directly applied to the DDS core [5]. Here we have to appropriately modify such a system into having 1-bit digital output (Fig. 10). We start by generating a high-quality carrier signal using a digital multi-bit-output phased-dithered DDS (a sine table is included but *not* a DAC) where phase-dithering is mainly used to reduce the size of the sine table. AM modulation is then implemented by directly multiplying the carrier with the data stream sequence.

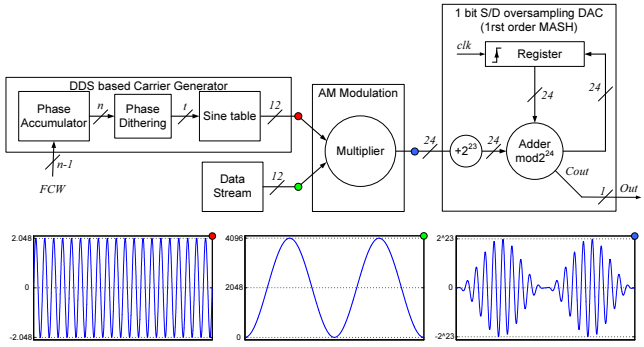

Figure 10. DDS based amplitude-multiplication AM modulation topology using a 1-bit output oversampling S/D DAC.

Up to this point we have generated the desired to transmit signal but it is in a multi-bit digital form and we want to avoid using a DAC (that the classic DDS topology uses).The problem is solved by using a purely digital, 1-bit output oversampling S/D modulator. The modulator can be of any order and type (low-pass or band-pass) but we recommend the use of the minimalistic solution of a first order (low-pass) S/D (MASH) modulator [7].

In general the output of such a simple S/D topology may result in a large number of strong undesirable spurs. In this scheme however some of the noise introduced by the phase-dithered carrier generator passes through the AM modulator and dithers the input of the S/D modulator. This way the near-in spurs are eliminated. A typical output spectrum of this technique is presented in Fig. 11. This minimalistic design can generate high quality signal of relative low frequency so this method is ideal for base-band signal generation.

The phase dithering sequence used in Carrier Generator is typically of *n-t* bits wide. Where *n* is the size of the phase accumulator and *t* the number of the bits that we keep after truncation (and so the address bus of the sine table). The value of *t* is selected based on the desired properties of the synthesizers output. A large *t* leads to larger sine table, lower phase dithering strength and lower noise floor of the output of the synthesizer but limits its spurs-free range to lower frequencies. Similarly a small *t* increases the output noise floor but enables the topology to generate higher frequencies. In some sense *t* should be chose according to with the desired oversampling ratio (F_{clk}/F_{out}).

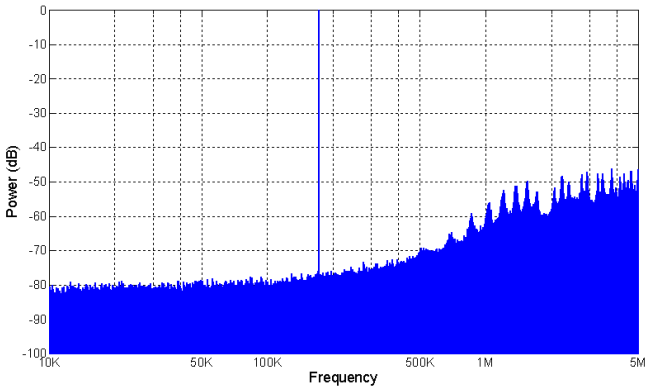

Figure 11. Spectrum of a dithered DDS core, using a 1-bit output oversampling S/D DAC (Matlab, f_{clk} = 10Mhz).

Finally, note that the core of this techniques is the phase dithered DDS in combination with a simple first-order S/D (MASH) modulator. It can be easily also without the AM modulator or combined with any other type of modulation applied to its DDS core.

IV. Live AM Radio Transmiter Demo

Based on the proposed architecture in section III.B and for the purpose of a live AM radio demonstration in the 2012 IFCS, the demo board of Fig. 12 was built. It is based on Xula-50 [8], a mini FPGA board that uses one of the smallest Xilinx FPGA chips of only 50k equivalent gates.

The implementation operated at 200MHz achieving noise floor of over 100dBc/Hz (within the desired frequency range).

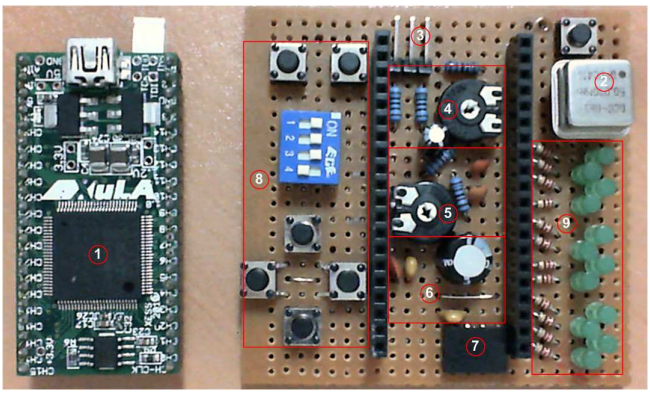

Figure 12. The board built for the perpouse of the Live Demo
1) Xula-50 mini FPGA Board
2) System clock generator
3) Analog audio input
4) Analog audio handling
5) ADC external analog parts
6) Power decoupling
7) Antenna connector
8) Configuration controls
9) LED Display (configuration and signal power meter)

A nearly all-digital 1-bit oversampling ADC was used to convert an external analog source into the digital data stream needed for the transmitter (Fig. 13). This is mostly a digital circuit only using a few passive analog components.

The analog source is connected to a resistor and capacitor network coupled to the digital circuit. The comparator unit is a simple CMOS inverter. The signal is sampled using a high frequency clock and then is low-pass flittered (using an IIR Filter) to produce the final *p*-bit wide digital data stream. This topology is able to sample baseband signals of relative low bandwidth with high resolution. It is a convenient method for sampling signals like audio or other analog sensor signals.

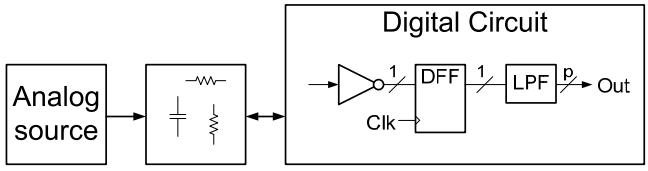

Figure 13. Basic topology of a 1-bit Oversampling ADC

Finally due to the large wave-length of AM radio band a simple loop antenna was used as the only practical option.

The FPGA utilization for this implementation is presented in Fig. 14. Despite this is a tiny FPGA chip, the transmitter occupies only about 40% of the total available recourses. Note that these numbers include the circuit of the ADC and various other circuits needed for having the live reconfigurability and LED display driving as well. The actual core of the transmitter (Synthesizer, Dithering and modulation as in Fig. 10) only uses about 20% of the available recourses. Finally we should note that only one of the FPGAs dedicated multipliers is used (needed by the selected AM modulation scheme).

AM Radio Demo (with ADC and controls)			
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice Flip Flops	404	1,408	28%
Number of 4 input LUTs	379	1,408	26%
Number of occupied Slices	304	704	43%

Figure 14. Device utilization of the implemented AM radio tramsiter.

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