PERSONAL INFORMATION	
SURNAME	PAPADOPOULOS
NAME	LAZAROS
DATE OF BIRTH	18.12.1980
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EDUCATION

09.2010 - 08.2016	School of Electrical and Computer Engineering, National Technical University of Athens, Greece. **PhD Degree**. Thesis: *Customization methodology of applications based on concurrent data structures in embedded systems.*
09.2005 - 06.2008	School of Electrical and Computer Engineering, Democritus University of Thrace. **MSc Degree.**
09.1999 - 06.2005	School of Electrical and Computer Engineering, Democritus University of Thrace. **Diploma of Electrical and Computer Engineering.**

RESEARCH/WORKING EXPERIENCE

01.2016 - Today	**Research associate in Microprocessors and Digital Systems Lab** of the School of Electrical and Computer Engineering of National Technical University of Athens. • Technical coordinator the European in H2020 project "**EXA2PRO**". Research and development in the area of application deployment in computing systems with heterogenous memories. • Research and Development in the context of the H2020 European project "**SDK4ED**", in the area of source-to-source memory management optimizations for improving energy efficiency.
10.2013 - 12.2015	**Visiting Researcher** at the Distributed Computing and Systems, Chalmers University of Technology, Sweden. • Research and development in the context of the FP7 European project "**EXCESS**", in the area of design and development of energy-aware concurrent data structures.
01.2009 – 10.2013	**Research associate in Microprocessors and Digital Systems Lab** of the School of Electrical and Computer Engineering of National Technical University of Athens. • Research and development in the context of the FP7 European project "**2PARMA**", in the area of real time memory management in embedded systems. • Research and development in the context of the FP7 European project "**MNEMEE**", in the area of memory management in embedded systems at design time.
03.2007 - 10.2007	**Visiting researcher in the European research center "Inter-university Micro Electronics Center"** (IMEC, Leuven, Belgium). Research in the implementation of application in Network-on-Chip-based architectures.

RESEARCH PROJECTS

Project Title	Funding source	Period	Role
PRAETORIAN: "Protection of Critical Infrastructures from advanced combined cyber and physical threats"	EU H2020	2021-2023	Research Associate
EXA2PRO: "Enhancing Programmability and Boosting Performance Portability for Exascale Computing Systems"	EU H2020	2018 – 2021	Technical Coordinator
SDK4ED: "Software Development Toolkit for Energy Optimization and Technical Debt Elimination"	EU H2020	2017 – 2020	Research Associate
EXCESS: Execution Models for Energy-Efficient Computing Systems	EU FP7	2013 - 2016	Research Associate
2PARMA: PARallel PAradigms and Run-time MAnagement techniques for Many-core Architectures	EU FP7	2009 - 2013	Research Associate
MNEMEE: Memory management technology for adaptive and efficient design of embedded systems	EU FP7	2008 - 2010	Research Associate

SELECTED PUBLICATIONS

- "**EXA2PRO: A Framework for High Development Productivity on Heterogeneous Computing Systems**", L. Papadopoulos, D. Soudris, C. Kessler, A. Ernstsson, J. Ahlqvist, N. Vasilas, A. Papadopoulos, P. Seferlis, C. Prouveur, M. Haefele, S. Thibault, A. Salamanis, T. Ioakimidis, D. Kehagias, IEEE TPDS, vol.33, no.4, 2021. link
- "**A Flexible Tool for Estimating Applications Performance and Energy Consumption Through Static Analysis**", C. Marantos, K. Salapas, L. Papadopoulos, D. Soudris, SN Computer Science 2(1): 21, 2021. link
- "**Portable exploitation of parallel and heterogeneous HPC architectures in neural simulation using SkePU**", S Panagiotou, A Ernstsson, J. Ahlqvist, L. Papadopoulos, C. Kessler, D. Soudris, SCOPES 2020. link
- "**A Design Space Exploration Framework for Convolutional Neural Networks implemented on Edge Devices**", F. Tsimpourlas, L. Papadopoulos, A. Bartsokas, D. Soudris, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (IEEE TCAD), 2018. link
- "**Efficient Winograd-based Convolution Kernel implementation on Edge Devices**", A. Xygkis, L. Papadopoulos, D. Moloney, D. Soudris, S. Yous, in Proc. 55th Annual Design Automation Conference (55th DAC), 2018. link
- "**A Systematic Methodology for Optimization of Applications Utilizing Concurrent Data Structures**", L. Papadopoulos, I. Walulya, P. Tsigas, D. Soudris, IEEE Trans. Computers 65(7), pp. 2019-2031, 2016. link
- "**Optimization methodology of dynamic data structures based on genetic algorithms for multimedia embedded systems**", C. Baloukas, J. L. Risco-Martín, D. Atienza, C. Poucet, L. Papadopoulos, S.

Mamagkakis, D. Soudris, J. I. Hidalgo, F. Catthoor, J. Lanchares, Journal of Systems and Software 82(4), pp. 590-602, 2009. link

- **"An automatic framework for dynamic data structures optimization in C",** C. Baloukas, L. Papadopoulos, R. Pyka, D. Soudris, P. Marwedel, VLSI-SoC 2010, pp. 155-160, 2010. link

CONFERENCES/WORKSHOPS/etc.

The list of the most recent conferences/workshops in which I participated:

- EoCoE – EXA2PRO joint workshop, 22-24 February 2021, virtual event. link
- HiPEAC 2021, 18-22 January 2021, virtual event. link
- SAMOS 2020, 4-8 July 2020, virtual event. link
- SCOPES 2020, 6-7 July, 2020, virtual event. link
- ESWEEK 2018, 30 Sept. – 5 Oct. 2018, Torino, Italy. link
- DAC 2018, June 2018, San Francisco, USA. link
- SCOPES 2018, July 2018, virtual event. link

FELLOWSHIPS and AWARDS

2015 **HiPEAC Collaboration Grant**, which supported the research visit in Chalmers University of Technology, Sweden.

2007 **IC-SAMOS best paper award** for the publication titled: "Systematic Data Structure Exploration of Multimedia and Network Applications realized Embedded Systems", L. Papadopoulos, C. Baloukas, N. Zompakis, D. Soudris, pp.58-65, 2007.

MEMBERSHIPS & REVIEWING ACTIVITIES

2015 - Today Member of the "**HiPEAC - European Network on High Performance and Embedded Architecture and Compilation**". link