A PARAMETERIZED GENETIC ALGORITHM IP CORE DESIGN AND IMPLEMENTATION

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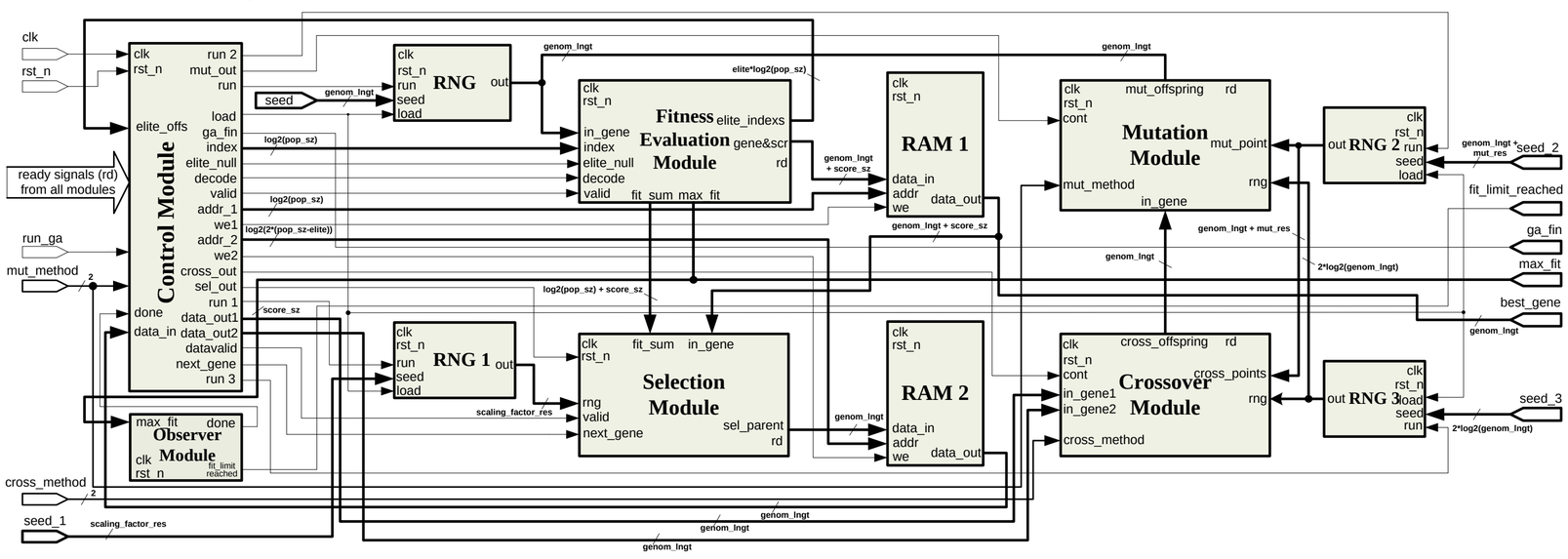
Introduction

A parameterized GA IP core is designed and implemented on hardware, achieving impressive time–speedups when compared to its software version. The parameterization stands for the number of population individuals and their bit resolution, the bit resolution of each individual's fitness, the number of elite genes in each generation, the crossover and mutation methods, the maximum number of generations, the mutation probability and its bit resolution. The proposed architecture is implemented in an Spartan 3-1500 FPGA chip with the use of VHDL and advanced synthesis and place and route tools. The designed GA IP core achieves a frequency rate of 92 MHz and is evaluated using the Traveling Salesman Problem (TSP) where a successful solution to it has been found, as well as several benchmarking functions.

Technological Approach

Overall System Architecture

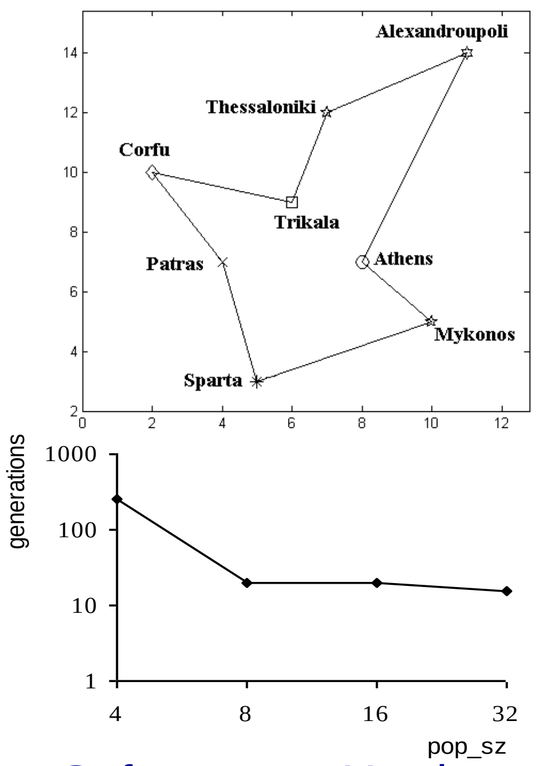


System sub-blocks

- Control Module
- Fitness Evaluation Module
- Selection Module
- Crossover Module
- Mutation Module
- Observer Module
- Random Number Generators
- Random Access Memory (RAM)

Experimental Results

TSP Evaluation: Map of the cities used, Population size vs. Generations



Software vs. Hardware

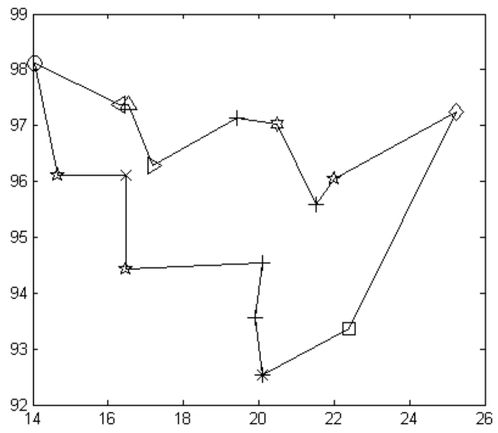
GA Version	Time(msec)
Hardware (11 nsec)	1,702
Software (Pentium 4 3,2 GHz 1Gb RAM)	18.783

IP Core Parameters

A GA IP core was developed with the following characteristics

Parameter name	Description	Possible Value
genom_lngt	Chromosome length in bits	16
score_sz	Fitness value bit resolution	16
pop_sz	Population size	32
scaling_factor_res	Bit resolution of the random number used in RWS algorithm	4
elite	Number of elite children	2
mr	Mutation rate	80

Solution of the **burma14** benchmark



FPGA Design Summary

Utilization of the implemented GA

Logic Utilization	GA	GA adapted to the TSP
Slice Flip Flops	681 (2%)	1045 (3%)
4 input LUT's	1.086 (4%)	1630 (6%)
Logic distribution		
Occupied Slices	892 (6%)	1305 (9%)
4 input LUT's	1.116 (6%)	1686 (6%)
Used as logic	1.086	1630
Used as route-thru	6	4
Used as 16x1 RAMs	24	52
Bonded IOBs	59 (12%)	53 (10%)
MULT 18x18s	1 (3%)	3 (9%)
GCLKs	1 (12%)	1 (12%)

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